Application Note

Third Party Flash Programming Support for the Z8 Encore!® MCU

AN011706-0608

Abstract

This Application Note provides an overview of the Flash Memory and Flash Controller in Zilog's Z8 Encore!® family of microcontrollers. It also describes a method to bypass the Flash Controller. The Flash Controller can be bypassed to allow direct control of Flash signals via the General-Purpose Input/Output (GPIO) pins.

The Flash Memory can be programmed faster by controlling the Flash Memory signals directly and is beneficial when programming a large number of devices. This method is used by third party vendors who manufacture using gang programmers.

Flash Memory Overview

Zilog's Z8 Encore! family of microcontrollers feature Flash Program Memory selections up to 64KB. By using Flash Memory, you have the ability to easily update the code. The Z8 Encore! MCU features an on-chip Flash Controller that manages the timing of Flash control signals for programming, Page Erase, and Mass Erase operations. For more information on Flash Memory and Flash Controllers, refer to the Z8 Encore! device-specific product specification.

Bypassing the Flash Controller

Flash Controller BYPASS mode is enabled by writing three bytes (`0x80`, `0xF0`, and `0x04`) to the On-Chip Debugger (OCD) through the DBG interface.

These three bytes are:

0x80—initiates an auto-baud calculation of the DGB interface data and clock rate.

0xF0—OCD Write Testmode Register command.

0x04—Data to be written to the Testmode Register enables Flash Controller BYPASS mode.

For more information on the On-Chip Debugger, refer to the Z8 Encore! device-specific product specification.

Flash Memory Control Signals

Depending on the size of (number of bytes available) Flash Memory, interfacing directly to Flash Memory uses 42 signals:

- 16 signals for the address lines
- 8 signals for data input
- 8 signals for data output
- 10 control signals

Table 1 on page 2 lists the Flash Memory control signals.

Table 1. Flash Memory Control Signals

Signal	Direction	Description
XADDR[9:0]	IN	X address input selects row. XADDR[9:0] corresponds to the upper 10 bits of the Program Memory address space (PROGMEM[15:6]). For Z8 Encore! devices with less than 64 KB of Program Memory, the unused upper address bits must be set to 0.
YADDR[5:0]	IN	Y address input selects one byte within a row. YADDR[5:0] corresponds to the lower 6 bits of the Program Memory address space (PROGMEM[5:0]).
DIN[7:0]	IN	Data input.
DOUT[7:0]	OUT	Data output.
XE	IN	X address enable.
YE	IN	Y address enable.
SE	IN	Sense amplifier enable.
OE	IN	Output enable.
ERASE	IN	Erase enable. This signal is used to select an erase operations.
MAS1	IN	Mass erase select. This signal is used to distinguish between Page Erase and Mass Erase operations.
PROG	IN	Program enable. This signal is used to select a program operation.
NVSTR	IN	Non-volatile store enable. This signal is used during Page Erase, Mass Erase, and programming operations.
TEST1	IN	This signal is used for test during manufacture of the part. This signal must be set to one during all operations.
TEST0	IN	This signal is used for test during manufacture of the part. This signal must be set to zero during all operations.

Flash Memory Operations

When bypassing the Flash Controller, all Flash Memory operations (Read, Program, Page Erase, and Mass Erase) are available. The mode of operation is set by the Flash Memory control signals as described in Table 2 on page 3.

Flash Bypass Mode Register Structure

To facilitate using Flash Controller BYPASS mode for all package sizes, all signals are registered internally. As a result, all data access is allowed to occur through a single 8-bit GPIO port (Port A). Three other GPIO port pins, (Ports B1, B0, and C0) select an data input register or data output register (see Table 3 on page 3).

Table 2. Flash Mode Truth Table

Mode	XE	YE	SE	OE	PROG	ERASE	MAS1	NVSTR	TEST1	TEST0
Read	H	H	H	H	L	L	L	L	H	L
Program	H	H	L	L	H	L	L	H	H	L
Page Erase	H	L	L	L	L	H	L	H	H	L
Mass Erase	H	L	L	L	L	H	H	H	H	L

Table 3. Control Registers in Flash Bypass Mode

	Register Select [Port B1, Port B0, Port C0]						
	000	001	010	011	100	101	110–111
Input/Output	Input	Input	Input	Input	Input	Output	Input
Port A7	XADDR[9]	XADDR[1]	DIN[7]	XE	TEST1	DOUT[7]	NOP
Port A6	XADDR[8]	XADDR[0]	DIN[6]	YE	TEST0	DOUT[6]	NOP
Port A5	XADDR[7]	YADDR[5]	DIN[5]	SE	NOP	DOUT[5]	NOP
Port A4	XADDR[6]	YADDR[4]	DIN[4]	OE	NOP	DOUT[4]	NOP
Port A3	XADDR[5]	YADDR[3]	DIN[3]	ERASE	NOP	DOUT[3]	NOP
Port A2	XADDR[4]	YADDR[2]	DIN[2]	PROG	NOP	DOUT[2]	NOP
Port A1	XADDR[3]	YADDR[1]	DIN[1]	MAS1	NOP	DOUT[1]	NOP
Port A0	XADDR[2]	YADDR[0]	DIN[0]	NVSTR	NOP	DOUT[0]	NOP

Flash Bypass Mode Register Structure

Figure 1 displays the multiplexed register structure that allows access to all Flash Memory signals through GPIO Port A.

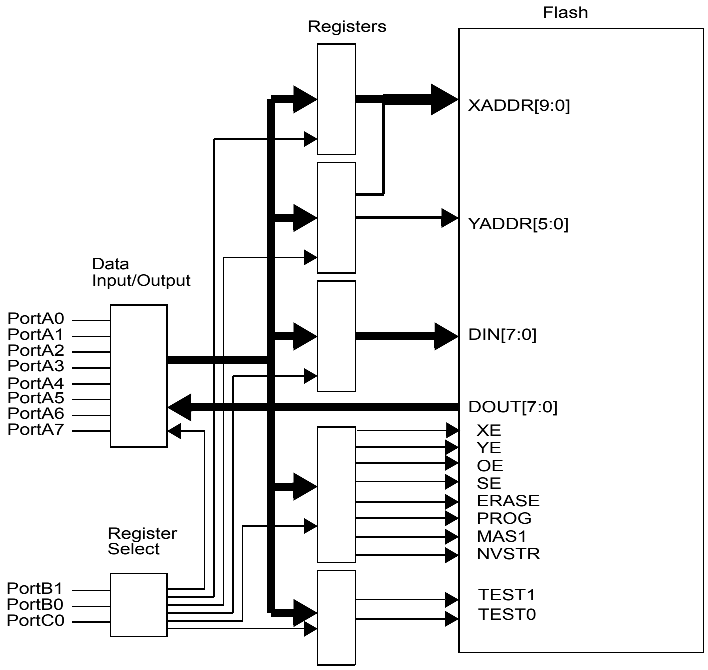


Figure 1. Flash Bypass Mode Register Structure

Bypass Mode Register Read Timing

Figure 2 displays the timing of a Read operation from the Flash Controller Bypass mode registers. When reading data, output data is latched into the output register on the first clock edge. The data is read on the next clock edge.

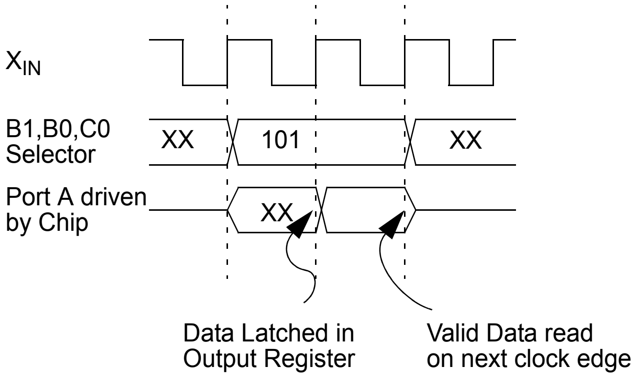


Figure 2. Bypass Mode Register Read Timing

Bypass Mode Register Write Timing

Figure 3 displays the timing of a write operation from the Flash Controller Bypass mode registers.

When writing data into the registers, the data is latched in on the rising edge of X_{IN}.

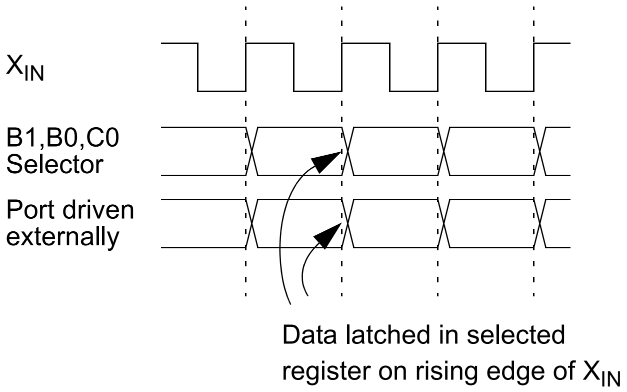


Figure 3. Bypass Mode Register Write Timing

Flash Row Programming

Flash Memory can be programmed either a single byte at a time or a row at a time. Multi-byte row programming allows programming of a full row of Flash Memory without incurring all of the programming setup and recovery time for each byte. During row programming, the Flash Memory's PROG and NVSTR signals are continuously asserted until all bytes in a row have been programmed. As a result, the row can be programmed more quickly than if these signals are deasserted after each byte is programmed.

During row programming, you must ensure that the cumulative programming high voltage period does not exceed the specification limits for a row. Zilog® recommends that row programming must be used onlyone time per row and not in combination with single-byte writes to the same row
without first erasing it.

Flash Memory Timing

Table 4, and Figure 4 through Figure 7, provide detailed timing information on accessing Flash Memory in Flash Controller BYPASS mode.

Table 4. Flash Memory Timing Parameters

Parameter	Symbol	Min	Max	Unit
X address access time	Txa	—	45	ns
Y address access time	Tya	—	45	ns
OE access time	Toa	—	4	ns
PROG/ERASE to NVSTR setup time	Tnvs	5	—	µs
NVSTR hold time	Tnvh	5	—	µs
NVSTR hold time (Mass Erase)	Tnvh1	100	—	µs
NVSTR to program setup time	Tpgs	10	—	µs
Program hold time	Tpgh	20	—	ns

Table 4. Flash Memory Timing Parameters (Continued)

Parameter	Symbol	Min	Max	Unit
Program time	Tprog	30	40	µs
Address / Data setup time	Tads	20	—	ns
Address / Data hold time	Tadh	20	—	ns
Recovery time	Trcv	1	—	µs
Cumulative program high voltage period[1]	Thv	—	8	ms
Erase time	Terase	10	—	ms
Mass Erase time	Tme	200	—	ms

Note: [1] Thv is the cumulative high voltage programming time for a single row before the next erase.

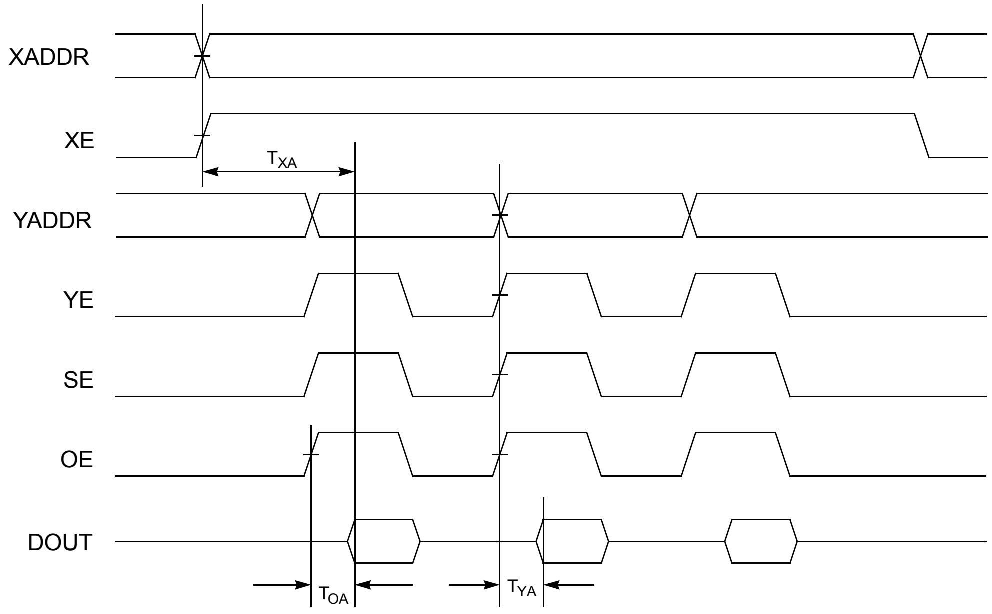
⚠ **Caution:** *The same address (byte) cannot be programmed more than twice before the next erase.*

Flash Read Timing

Figure 4 displays the timing of a Read operation from Flash Memory.

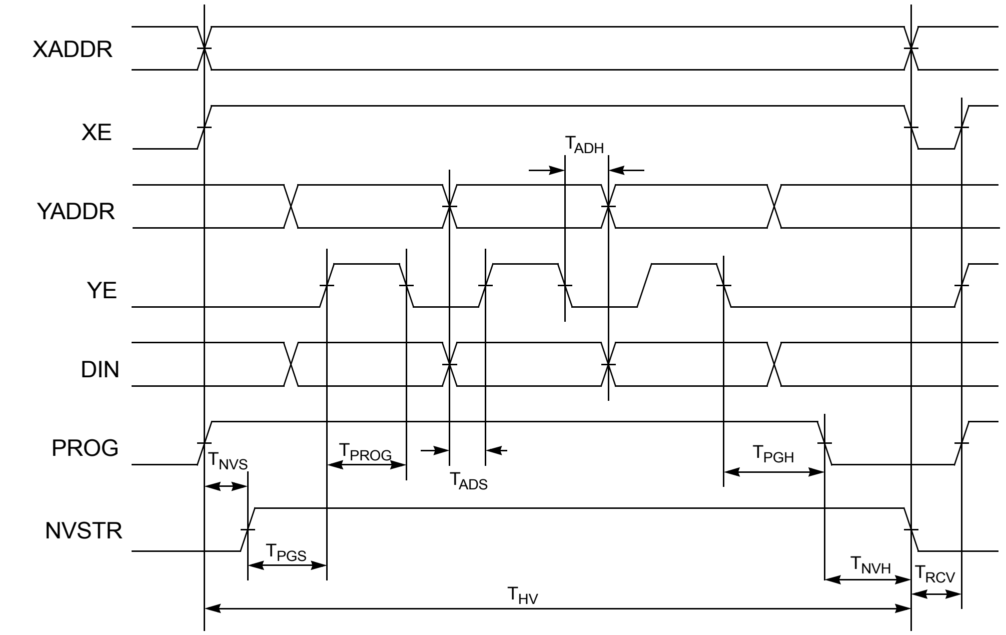
Flash Program Timing

Figure 5 on page 7 displays the Flash programming operation for 3 Bytes on a single row. XADDR remains unchanged while PROG is High, but YADDR changes 3 times to identify 3 different bytes in a single row.



ERASE = 0, MAS1 = 0, NVSTR = 0, TEST1 = 1, TEST0 = 0

Figure 4. Flash Read Timing

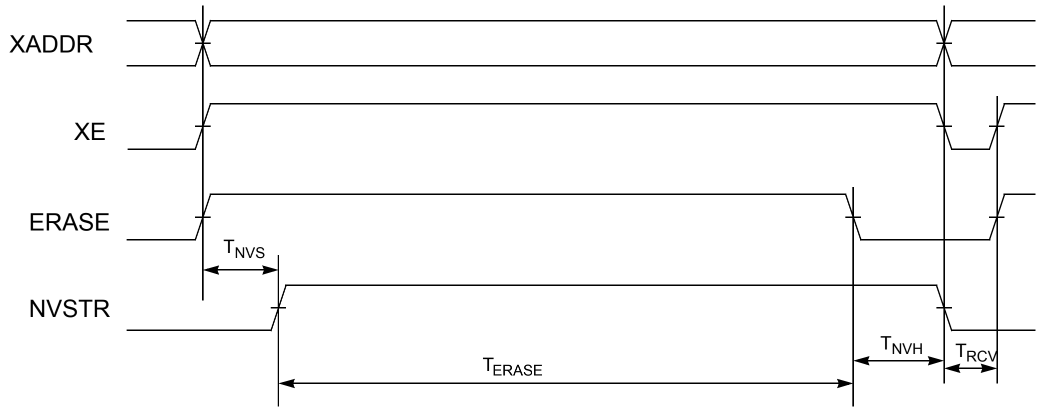


SE = 0, OE = 0, ERASE = 0, MAS1 = 0, TEST1 = 1, TEST0 = 0

Figure 5. Flash Byte Program Timing

Flash Page Erase Timing

Figure 6 displays the timing of a Flash Page Erase operation.

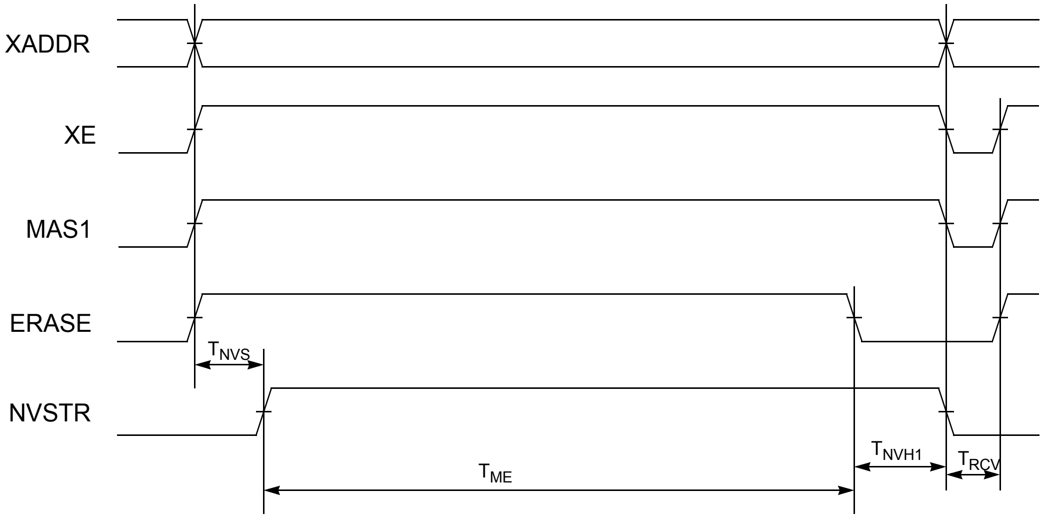


YE = 0, SE = 0, OE = 0, PROG = 0, MAS1 = 0, TEST1 = 1, TEST0 = 0

Figure 6. Flash Page Erase Timing

Flash Mass Erase Timing

Figure 7 displays the timing of a Flash Mass Erase operation.



YE = 0, SE = 0, OE = 0, PROG = 0, TEST1 = 1, TEST0 = 0

Figure 7. Flash Mass Erase Timing

Z8F04xA XP Flash Programming Flowchart

Figure 8 displays an example flowchart for Read and Write operations.

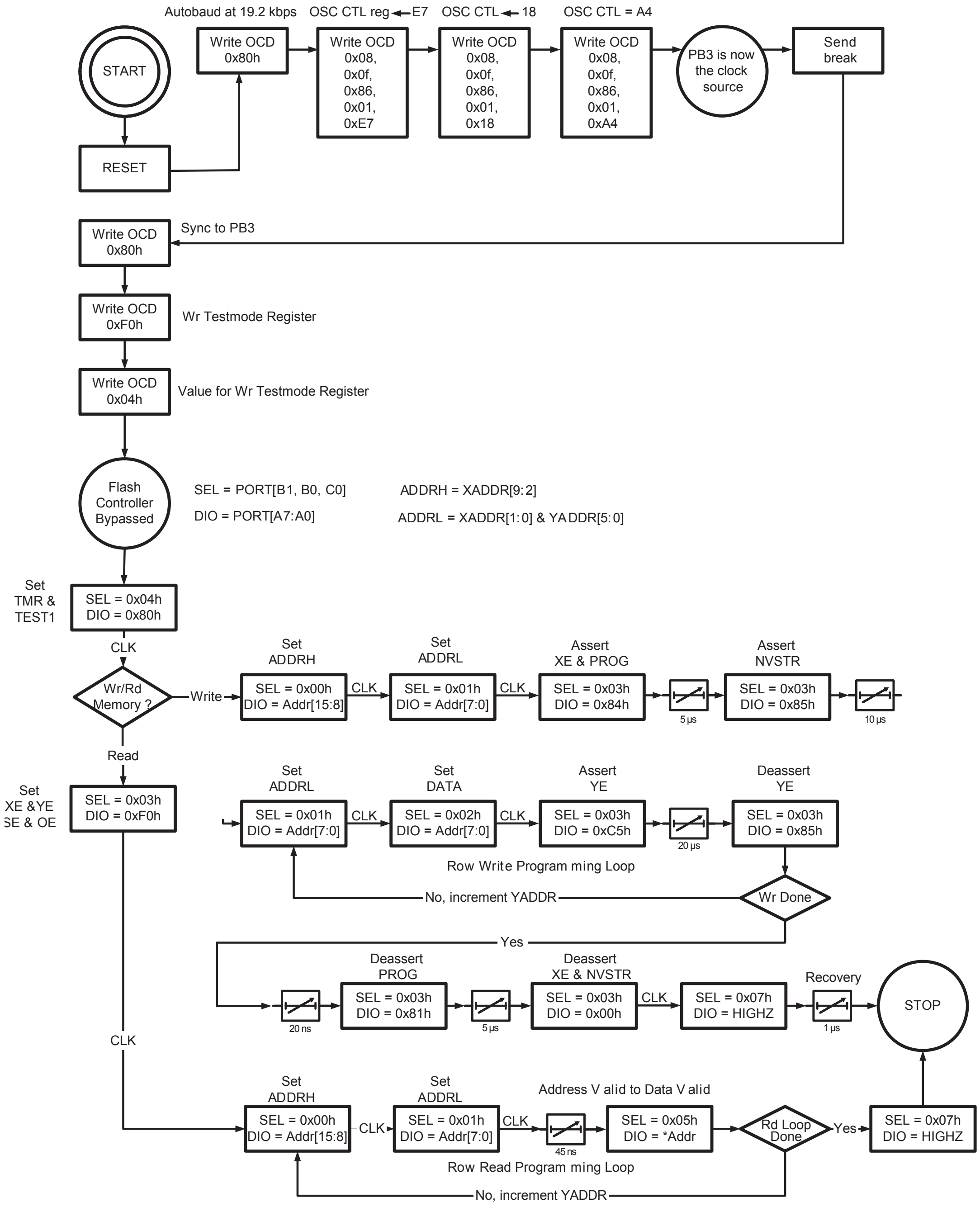


Figure 8. Z8F04xA XP Flash Gang Programming Flow

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